REMARKS/ARGUMENTS

The Examiner states that claims 1 and 3--9 remain rejected under 35 U.S.C. §102(b) as being anticipated by Kaplinsky of record. The Examiner states that claims 2 and 10 are objected to as being dependent upon a rejected base claim, but will be allowable if rewritten in independent form including all limitations of the base claim and any intervening claims. Accordingly, claims 1 and 2 have been combined to produce a new Claim 2 and claims 7 and 10 have been combined to produce a new claim 10. Claims 3, 4 and 6 have been amended to be dependent upon new Claim 2. Claim 8 has been amended to become dependent upon new Claim 10 which should render claims 3-9 allowable. The Examiner has allowed claims 11-13 and 15-16.

With respect to Claims 1 and 7, the Examiner states that, in response to Applicant's arguments that Kaplinsky does not anticipate the limitation that "output signals at UOP and LOP in response to an input signal at IN such that during an input transition IN, the UOP and LOP are never on simultaneously" as recited in claims 1 and 7 are not persuasive. The Examiner refers Applicants to Col. 2, Lines 45-55 of Kaplinsky which he says explicitly states that the pass gates allow only one of the two inverters to have active control of the pair of output transistors at any one time whenever the input signal is in transition. The Examiner concludes that the limitation of having the UOP and LOP never on simultaneously is fully met.

Applicants agree with the Examiner that Kaplinsky stands for having only one of the two inverters coupled via the pass gates to the pair of output transistors at any one time. In fact, that is exactly why Kaplinsky can not work in the manner of the present invention. In Kaplinsky, inverter (42) of FIGURE 2 is used to control the pull-down operation. This means as the input signal transitions lower, the output of inverter (42) will transition higher, which will be connected to the gate of NMOS transistor (52), thus turning the transistor on. However, the same signal on line (44), will be connected to the gate of PMOS transistor (51) thereby turning it off. However, as the output voltage

on line (44) increase, transistor (52) will gradually turn on while transistor (51) will gradually turn off. At some point, both transistors will be in the on state, thus allowing current to flow from the voltage supply V_{DD} to the reference supply V_{SS}, which is known as the short circuit current in the present application. It is just this short circuit current that the present invention seeks to avoid. The only way this can be accomplished, is to drive the gates of the transistors (51), (52), in opposite directions so they will both be turned off to avoid the short circuit current. In view of the fact, that the Examiner has stated that the gates of transistors (51) and (52) are connected to one or the other inverter (41), (42) together, Kaplinsky can not ever accomplish this feat, and in fact, teaches away from the present invention by coupling both gates to the same signal source.

Claims 1 and 7 have been amended in order to more clearly recite this feature by reciting a control electrode for the UOP and the LOP are driven toward opposite voltage supplies so that the UOP and the LOP are never on simultaneously. This feature clearly distinguishes claims 1 and 7 from the Kaplinsky reference.

Accordingly, Applicants believe that the Application, as amended, is in condition for allowance, and such action is respectfully requested.

Respectfully submitted,
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